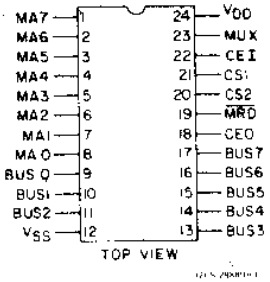
CDP1833, CDP1833C Types

1024-Word x 8-Bit Static Read-Only Memory

Features:

- Compatible with CDP1800-series microprocessors
- Static CMOS circuitry—CD4000-series compatible
- Interfaces with CDP1802 and CDP1804 microprocessors without additional components
- Fast access time: 350 ns typ. at V_{DD}=10 V
- Single voltage supply
- On-chip address latch
- 3-state outputs
- Operating temperature range—
  —55 to +125°C (CDP1833D, CDP1833CD) —40 to +85°C (CDP1833E, CDP1833CE)
- Low quiescent and operating power



Terminal Assignment

The RCA-CDP1833 and CDP1833C are static 8192-bit mask-programmable COS/MOS read-only memories organized as 1024-words x 8 bits and designed for use in CDP1800-series microprocessor systems. They will directly interface with the CDP1802 and CDP1804 microprocessors without additional components.

The CDP1833 and CDP1833C respond to 16-bit address multiplexed on 8 address lines. Address latches are provided on-chip to store the 8 most significant bits on the 16-bit address. By mask option, this ROM can be programmed to operate in any 1024-word byte of 64K memory space. (See PD30, "ROM Purchase Policy and Data Programming Instructions".) Two Chip-Select inputs are also provided.

The polarity of MUX(TPA), CEI, CS1 and CS2 are user mask-programmable. The Chip-Enable output signal (CEO) is "high" with coincidence of Address CS1, CS2 and CEI. Terminals CEO and CEI can be connected in a daisy chain to control selection of RAM chips in a microprocessor system without additional components.

The CDP1833C is functionally identical to the CDP1833. The CDP1833 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1833C has a recommended operating voltage range of 4 to 6.5 volts.

The CDP1833 and CDP1833C are supplied in 24-lead hermetic dual-in-line side-brazed ceramic package (D suffix) and 24-lead dual-in-line plastic package (E suffix).

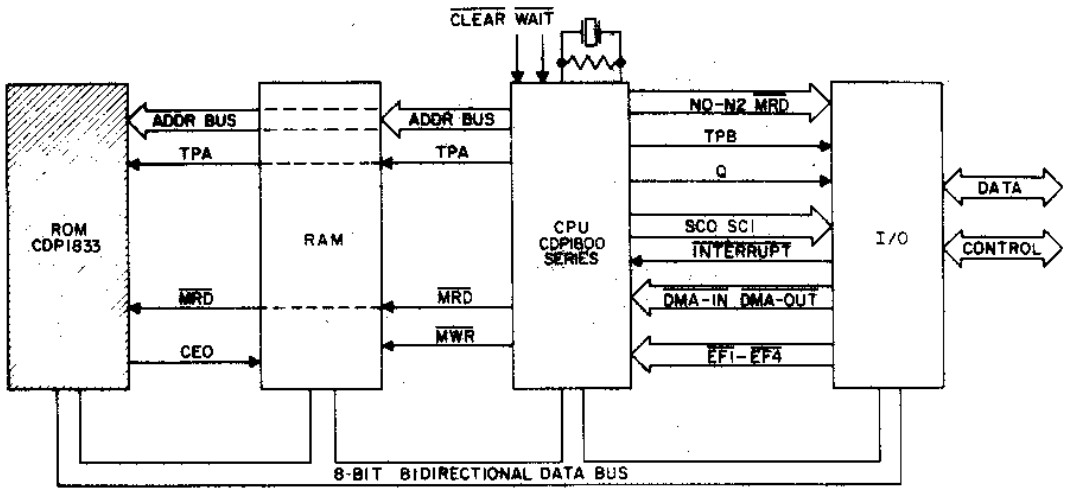


Fig. 1 — Typical CDP1800 Series microprocessor system.

CDP1833

CDP1833, CDP1833C Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(All voltage values referenced to V_{SS} terminal)

CDP1833	−0.5 to +11 V
CDP1833C	−0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPE D)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE	100 mW
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPE D	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

OPERATING CONDITIONS at T_A = Full Package Temperature Range

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

CHARACTERISTIC	LIMITS				UNITS
	CDP1833		CDP1833C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

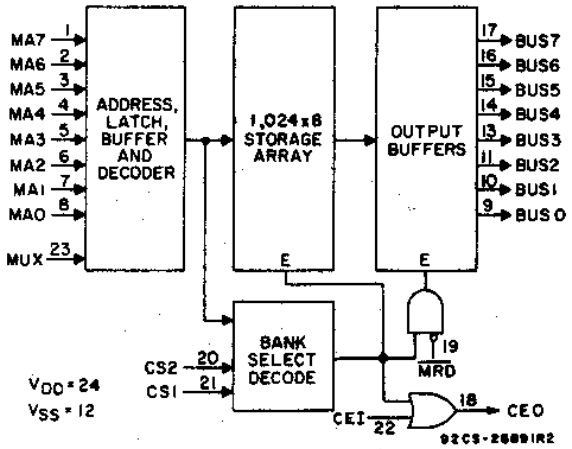


Fig. 2 — Functional diagram.

CDP1833, CDP1833C Types

STATIC ELECTRICAL CHARACTERISTICS at T_A = –40 to +85°C, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1833D CDP1833E			CDP1833CD CDP1833CE			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_L	–	5	5	–	0.01	50	–	0.02	200	μA
	–	10	10	–	1	200	–	–	–	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	0.8	–	–	0.8	–	–	mA
	0.5	0,10	10	1.8	–	–	–	–	–	
Output High Drive (Source Current) I_{OH}	4.6	0,5	5	–0.8	–	–	–0.8	–	–	mA
	9.5	0,10	10	–1.8	–	–	–	–	–	
Output Voltage Low-Level V_{OL}	–	0,5	5	–	0	0.05		0	0.05	V
	–	0,10	10	–	0	0.05	–	–	–	
Output Voltage High Level, V_{OH}	–	0,5	5	4.95	5	–	4.95	5	–	
	–	0,10	10	9.95	10	–	–	–	–	
Input Low Voltage V_{IL}	0.5,4.5	–	5	–	–	1.5	–	–	1.5	V
	1,9	–	10	–	–	3	–	–	–	
Input High Voltage V_{IH}	0.5,4.5	–	5	3.5	–	–	3.5	–	–	
	1,9	–	10	7	–	–	–	–	–	
Input Leakage Current I_{IN}	Any Input	0,5	5	–	$\pm 10^{-4}$	±1	–	$\pm 10^{-4}$	±1	μA
		0,10	10	–	$\pm 10^{-4}$	±2	–	–	–	
3-State Output Leakage Current I_{OUT}	0,5	0,5	5	–	$\pm 10^{-4}$	±1	–	$\pm 10^{-4}$	±1	μA
	0,10	0,10	10	–	$\pm 10^{-4}$	±2	–	–	–	

*Typical values are for T_A = 25°C and nominal V_{DD}.

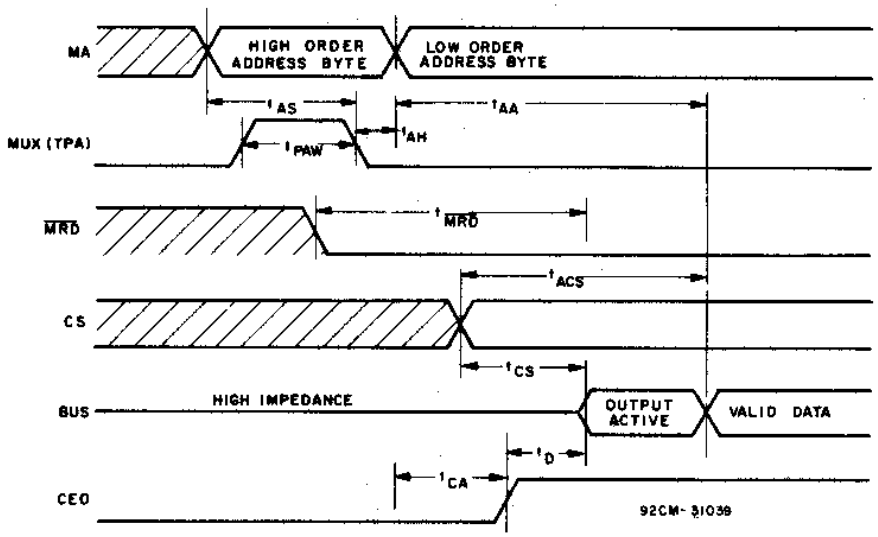


Fig. 3 – Timing diagram.

CDP1833, CDP1833C Types

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DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ±5%, Input t_r, t_f = 10 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS						UNITS
		CDP1833			CDP1833C			
		Min.#	Typ.●	Max.	Min.#	Typ.●	Max.	
Access Time from Address Change, t_{AA}	5	–	650	775	–	650	775	ns
	10	–	350	425	–	–	–	
Access Time from Chip Select, t_{ACS}	5	–	500	625	–	500	625	ns
	10	–	275	310	–	–	–	
Chip Select Delay, t_{CS}	5	–	250	320	–	250	320	ns
	10	–	125	180	–	–	–	
Address Setup Time, t_{AS}	5	75	50	–	75	50	–	ns
	10	40	25	–	–	–	–	
Address Hold Time, t_{AH}	5	100	75	–	100	75	–	ns
	10	50	30	–	–	–	–	
Read Delay, $t_{\overline{MRD}}$	5	–	400	500	–	400	500	ns
	10	–	200	275	–	–	–	
Chip Enable Output Delay from Address, t_{CA}	5	–	120	170	–	120	170	ns
	10	–	70	100	–	–	–	
Bus Contention Delay, t_D	5	–	220	270	–	220	270	ns
	10	–	130	150	–	–	–	
MUX Pulse Width (TPA), t_{PAW}	5	200	–	–	200	–	–	ns
	10	70	–	–	–	–	–	
Dynamic Power Dissipation P_D (cycle time = 2.5 μs)	5	–	30	–	–	30	–	ns
	10	–	120	–	–	–	–	

#Time required by a limit device to allow for the indicated function.

●Time required by a typical device to allow for the indicated function. Typical values are for T_A = 25°C and nominal voltages.

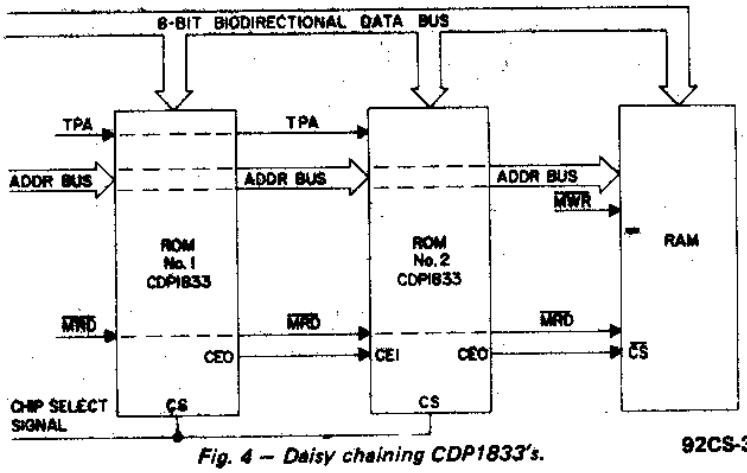

Fig. 4 – Daisy chaining CDP1833's.

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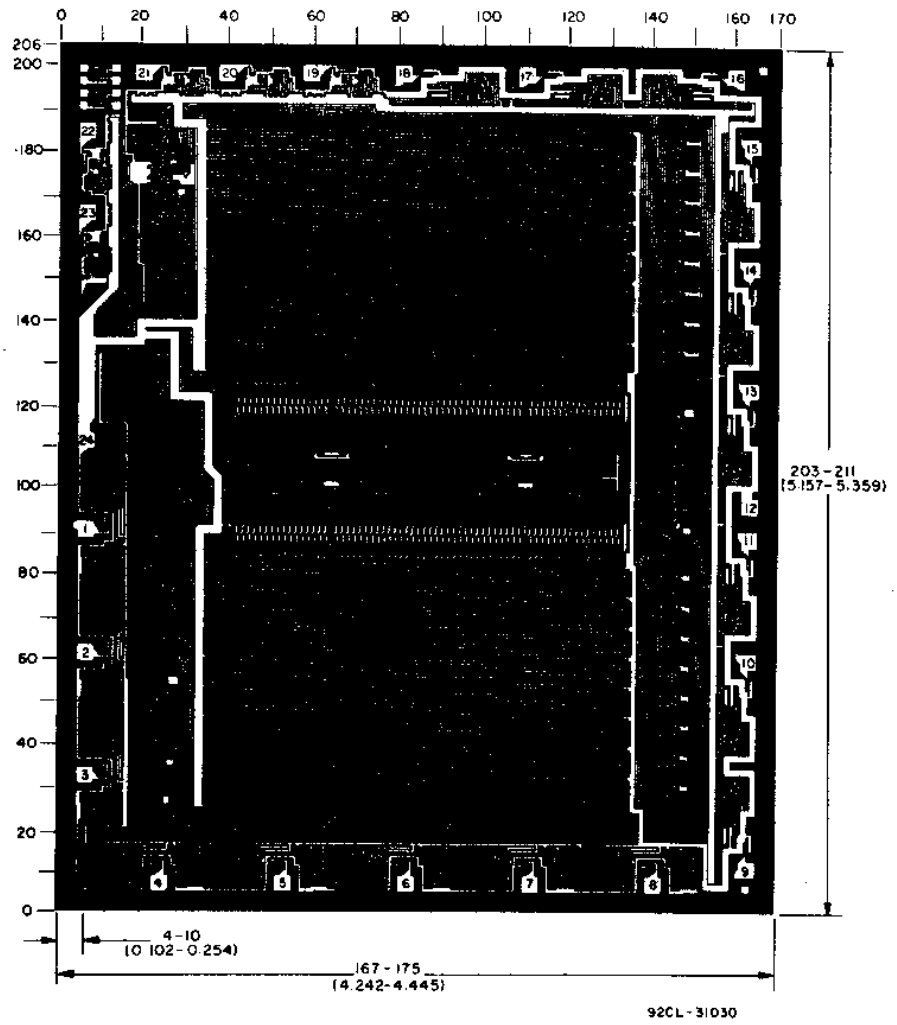
"Daisy Chaining" with CEI inputs and CEO outputs is used to avoid memory conflicts between ROM and RAM in a user system. In the above configuration, if ROM #1 was masked-programmed for memory locations 000-03FF$_{16}$ and ROM #2 masked-programmed for memory locations 0400$_{16}$-07FF$_{16}$, for addresses from 0000-07FF$_{16}$ the RAM would be disabled and the ROM enabled. For locations above 07FF$_{16}$ the ROM's would be disabled and the RAM enabled.

CDP1833, CDP1833C Types



Dimensions and pad layout for CDP1833 chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Note:
The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1833. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1833 is used with the CDP1802 or CDP1804 microprocessor.

$t_{AH} = 0.5\ t_C$
$t_{PAW} = 1.0\ t_C$
MRD occurs one clock period (t_C) earlier then the adress bits MA0-MA7.

where $t_C = \frac{1}{\text{CPU clock frequency}}$

The CDP1833 is capable of operating at the maximum clock frequency of the CDP1802 or CDP1804 microprocessor.